a first dielectric layer disposed between the plurality of the active regions and the plurality of the first gates, and between the plurality of the active regions and the plurality of the second gates;

a second dielectric layer disposed between the plurality of the word lines and the plurality of the first gates, and between the plurality of the source lines and the plurality of the second gates;

a third dielectric layer disposed over the substrate and covering the plurality of the word lines and the plurality of the source lines;

a plurality of source/drain regions disposed in the active regions beside the first gates and the second gates;

a plurality of source line contacts, through the third dielectric layer, connecting to the source/drain regions that are between each pair of the source lines and electrically connecting to at least one of each pair of the source lines; and

a plurality of insulating layers disposed between the plurality of the second gates and the plurality of the source line contacts.

2. (original) The memory device of claim 1, wherein the plurality of the isolation structures, substantially parallel to one another, are disposed in the substrate and are in strip shapes, thus defining the plurality of active regions in strip shapes.

3. (original) The memory device of claim 1, wherein a height of the source lines disposed above the second gates is between a height of the second gates and a height of the word lines.

4. (original) The memory device of claim 3, wherein the height of the source lines

disposed above the second gates is substantially the same as the height of the word lines.

5. (original) The memory device of claim 1, wherein a material of the source lines is the same as that of the word lines.

6. (original) The memory device of claim 1, wherein a material of the source lines includes polysilicon and metal silicide, while a material of the word lines includes polysilicon and metal silicide.

7. (original) The memory device of claim 1, further comprising a plurality of spacers, disposed between the word lines and the source lines neighboring to the word lines, and wherein a thickness of the insulating layer between the second gate and the source line contact is smaller than a half of a thickness of the spacer.

8. (original) The memory device of claim 1, wherein each source line contact connects to one source/drain region in one active region between each pair of the source lines and connects to at least one of each pair of the source lines.

9. (original) The memory device of claim 1, wherein each source line contact connects to at least two source/drain regions in at least two adjacent active regions between each pair of the source lines and connects to at least one of each pair of the source lines.

10. (original) The memory device of claim 1, wherein each source line contact is a self-aligned contact.

11. (original) The memory device of claim 1, further comprising a plurality of bit line contacts, through the third dielectric layer, connecting the source/drain regions beside each pair of the word lines, and wherein a height of the bit line contacts is substantially the

same as a height of the source line contacts.

12. (original) The memory device of claim 1, wherein when the memory device is a flash memory device, the first gate is a floating gate and the second gate is a select gate.

13. (original) A memory device, disposed in a substrate, the memory device comprising a plurality of pairs of word lines, a plurality of pairs of source lines and a plurality of source/drain regions, wherein the memory device is characterized in that:

each pair of source lines, substantially parallel to each other and electrically connected to each other, is disposed between each pair of word lines, and the source/drain regions are disposed between each pair of source lines and between the source lines and the adjacent word lines, the word lines, the source lines and the source/drain regions are covered by a dielectric layer; and

a plurality of source line contacts, through the third dielectric layer, is further included, connecting to at least one of the source/drain regions that are between each pair of the source lines and electrically connecting to at least one of each pair of the source lines.

14. (original) The memory device of claim 13, wherein a height and a contour of the source lines are substantially equivalent to a height and a contour of the word lines.

15. (original) The memory device of claim 13, wherein a material of the source lines is the same as a material of the word lines.

16. (original) The memory device of claim 15, wherein the material of the source lines includes polysilicon and metal silicide, while the material of the word lines includes polysilicon and metal silicide.

17. (original) The memory device of claim 13, wherein the memory device is further characterized in that:

a plurality of isolation structures is disposed in the substrate and is in strip shapes, thus defining a plurality of active regions in strip shapes in the substrate; and

each source line contact connects to one source/drain region in one active region between each pair of the source lines and connects to at least one of each pair of the source lines.

18. (original) The memory device of claim 13, wherein the memory device is further characterized in that:

a plurality of isolation structures is disposed in the substrate and is in strip shapes, thus defining a plurality of active regions in strip shapes in the substrate; and

each source line contact connects to at least two source/drain regions in at least two adjacent active regions between each pair of the source lines and connects to at least one of each pair of the source lines.

19. (original) The memory device of claim 13, wherein each source line contact is a self-aligned contact.

20. (original) The memory device of claim 13, further comprising a plurality of bit line contacts, through the third dielectric layer, connecting the source/drain regions beside each pair of the word lines, and wherein a height of the bit line contacts is substantially the same as a height of the source line contacts.

21. (original) The memory device of claim 17, further comprising:

a plurality of first gates, disposed between the substrate and the word lines;

a plurality of second gates, in strip shapes, disposed on and in a direction vertical to the plurality of the strip isolation structures and the plurality of the active regions and disposed between the substrate and the source lines;

a first dielectric layer, disposed between the substrate and the plurality of the fist gates and between the substrate and the plurality of the second gates; and

a second dielectric layer, disposed between the plurality of the fist gates and the word lines and between the source lines and the plurality of the second gates.

22. (original) The memory device of claim 21, wherein when the memory device is a flash memory device, the first gate is a floating gate and the second gate is a select gate.

Claims 23-39 (canceled).